

**1.2 Gb, DDR - SDRAM Integrated Module (IMOD)**

**FEATURES**

- ❑ DDR SDRAM Data Rate = 200, 250, 266, and 333 Mbps
- ❑ Package:
  - 25mm x 25mm, Encapsulated Laminate Ball Grid array (LBGA), 219 balls, 1.27mm pitch.
- ❑ 2.5v ±0.2V Core Power supply
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- ❑ Differential Clock inputs (CLKx, CLKx)
- ❑ Commands entered on each positive CLKx edge
- ❑ Internal pipelined double-data-rate (DDR) Architecture; two data accesses per clock cycle
- ❑ Programmable Burst Length: 2, 4, or 8
- ❑ Bidirectional data strobe (DQSLx, DQsHx) per byte transmitted/received with data  
i.e. source-synchronous data capture
- ❑ DQS edge-aligned with data for READ; center-aligned with data for WRITE
- ❑ DLL to align DQx and DQSLx, DQSHx transitions with CLKx
- ❑ Four internal banks for concurrent operation
- ❑ One data mask per byte, IMOD contains (10) bytes
- ❑ Programmable IOL/IOH Option
- ❑ Auto PRECHARGE option
- ❑ Auto REFRESH and SELF REFRESH Modes
- ❑ Available in INDUSTRIAL, EXTENDED and Mil-Temp ranges
- ❑ Organized as 16M x 72/80
- ❑ Weight: LOGIC Devices, Inc. L9D112G80BG4 = 2.75 grams typical

**Benefits**

- ❑ 53% SPACE savings vs. Monolithic, TSOPII-66 solution
- ❑ Reduced I/O routing (34%)
- ❑ Reduced trace length providing improved/reduced parasitic capacitance
- ❑ Impedance matched (60ohm) packaging
- ❑ High TCE organic laminate interposer
- ❑ Suitable for High Reliability applications
- ❑ Upgradable to 32M x 72/80: L9D125G80BG4

*\*Note: This integrated product and/or its specifications are subject to change without notice.  
Latest document should be retrieved from LDI prior to your design consideration.*



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	MONOLITHIC SOLUTION	IMOD SOLUTION	
OPTIONS			SAVINGS
AREA	5 X 265mm <sup>2</sup> = 1328mm <sup>2</sup> PLUS	625mm <sup>2</sup>	53%
I/O	5 X 66 pins = 320 pins total	219 Balls/Locations	34%